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EXAMINER	
OSBORNE, LUKE R	
ART UNIT	**PAPER NUMBER**
2123	

MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/076,920	DELIWALA, SHRENIK	
	Examiner	Art Unit	
	Luke Osborne	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-57* is/are pending in the application.

4a) Of the above claim(s) *12-43,57* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *44-56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 February 2007* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

9/24/03
3/14/03
1/27/03

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date 3/15/02, 4/15/02, 11/1/02, 1/14/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 44-56 in the reply filed on 4/12/2007 is acknowledged.

Claims 12-43, 57 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to nonelected groups, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 4/12/2007.

Claim Status

2. Claims 12-57 are pending in the instant application.

Claims 44-56 stand rejected.

Claims 12-43, 57 are withdrawn from further consideration as being directed to a non-elected group of claims.

Domestic Priority

3. Applicant's claim for domestic priority under 35 U.S.C. 119(e) is acknowledged.

Information Disclosure Statement

4. The information disclosure statement (IDS) submissions on 2/15/02, 11/1/02, 1/14/03, 1/27/03, 3/14/03, 9/24/03 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

The Examiner has NOT considered the reference L listed on IDS submission on 3/14/2003 as no copy of the identified references was found with the submission.

The Examiner has NOT considered the references L, M, N, O, P and Q listed on IDS submission on 2/15/02 as no copy of the identified references was found with the submission.

The IDS submission on 4/15/02 is not in compliance with 37 CFR 1.98 a (ii), and is not being considered by the Examiner. The submission on 4/15/02 does not contain a proper listing of the references for consideration, also the Examiner can not find Exhibit A which is referenced in the submission. The Examiner will consider those references when submitted in accordance with 37 CFR 1.97 and 1.98, preferably listed on a new 1449.

Drawings

5. The drawings are objected to because they are deficient under the following sections of 37 CFR 1.84. Figures 1-91 are affected.

(l) Character of lines, numbers, and letters. All drawings must be made by a process which will give them satisfactory reproduction characteristics. Every line, number, and letter must be durable, clean, black (except for color drawings), sufficiently dense and dark, and uniformly thick and well-defined. The weight of all lines and letters must be heavy enough to permit adequate reproduction. This requirement applies to all lines however fine, to shading, and to lines representing cut surfaces in sectional views.

Lines and strokes of different thicknesses may be used in the same drawing where different thicknesses have a different meaning.

The hand drawn numbering of the all the drawing sheets and the reference numerals found in Figures 59, 60, 63D, 66, 73, 78-91 are unacceptable, as is any other hand markings in the drawings.

(t) Numbering of sheets of drawings. The sheets of drawings should be numbered in consecutive Arabic numerals, starting with 1, within the sight as defined in paragraph (g) of this section. These numbers, if present, must be placed in the middle of the top of the sheet, but not in the margin. The numbers can be placed on the right-hand side if the drawing extends too close to the middle of the top edge of the usable surface. The drawing sheet numbering must be clear and larger than the numbers used as reference characters to avoid confusion. The number of each sheet should be shown by two Arabic numerals placed on either side of an oblique line, with the first being the sheet number and the second being the total number of sheets of drawings, with no other marking.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure

is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

The newly submitted clean copy of the drawings should be as they were before the first Office Action, including any preliminary or other amendments. If any additional changes are required they should also be shown accordingly in a separate submission of marked up Figures.

Specification

6. A substitute specification excluding the claims is required pursuant to 37 CFR 1.125(a).

(a) If the number or nature of the amendments or the legibility of the application papers renders it difficult to consider the application, or to arrange the papers for printing or copying, the Office may require the entire specification, including the claims, or any part thereof, be rewritten.

It is difficult to determine the current content of the instant specification. The instant application contains two seemingly identical specifications submitted with the filling of the application on 2/15/2002. Also submitted with the filling of the application on 2/15/02 are what appears to be two preliminary amendments. In addition to the preliminary amendments there is a further amendment submitted on 3/7/04. The changes made to the specification are acceptable though difficult for consideration and Examination purposes, but would pose a significant challenge for printing or copying.

A substitute specification must not contain new matter. The substitute specification must be submitted with markings showing all the changes relative to the immediate prior version of the specification of record. The text of any added subject matter must be shown by underlining the added text. The text of any deleted matter must be shown by strike-through except that double brackets placed before and after the deleted characters may be used to show deletion of five or fewer consecutive characters. The text of any deleted subject matter must be shown by being placed within double brackets if strike-through cannot be easily perceived. An accompanying clean version (without markings) and a statement that the substitute specification contains no new matter must also be supplied. Numbering the paragraphs of the specification of record is not considered a change that must be shown.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 55 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 55 recites the limitation "the optical simulation design tools portion" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 44-49, 52-56 are rejected under 35 U.S.C. 102(b) as being anticipated by "Numerical Simulation of a Silicon-on-Insulator Waveguide Structure for Phase Modulation at 1.3um" by Adrian Vonsovici et al., hereinafter "Vonsovici".

Regarding claim 44, Vonsovici discloses a method of operating a computer processor, the computer processor using computer software, the computer software is configured to simulate the electrical characteristics and the optical characteristics of an integrated optical/electronic circuit, the method comprising:

generating topology information and free-carrier concentration information by simulating operation of a least certain electronic circuits of said integrated optical/electronic circuit using an electronic design portion [Vonsovici: The electrical

tuning of this FP interferometer is analyzed using electrical simulations of the carrier injection in the lateral P+/N /N+ diode (Page 2124, right column, last paragraph)], and

simulating operation of at least certain optical circuits of said integrated optical/electronic circuit in an optical design portion in response to said topology information and said free-carrier concentration information generated by said electronic design portion [Vonsovici: Finally, the modulation efficiency of the reflectivity is estimated using the results of the optical simulations and the estimated effective index change (Page 2125, left column, first paragraph)].

Regarding claim 45 Vonsovici discloses the method of claim 44, wherein the electronic design portion includes a process simulation portion that generates said topology information [Vonsovici: The electrical tuning of this FP interferometer is analyzed using electrical simulations of the carrier injection in the lateral P+/N /N+ diode (Page 2124, right column, last paragraph)].

Regarding claim 46 Vonsovici discloses the method of claim 44, wherein the electron design portion includes a device simulation portion that generates said free-carrier concentration information [Vonsovici: The electrical tuning of this FP interferometer is analyzed using electrical simulations of the carrier injection in the lateral P+/N /N+ diode (Page 2124, right column, last paragraph)].

Regarding claim 47 Vonsovici discloses the method of claim 44, wherein said electronic design portion includes at least one of the group consisting of a process simulation portion, a device simulation portion, a layout portion, a parasitic extraction portion, and a circuit simulation portion [Vonsovici: Figure 2, page 2125, The electrical tuning of this FP interferometer is analyzed using electrical simulations of the carrier injection in the lateral P+/N /N+ diode. A perturbation analysis is used to determine the effective index modulation as a function of the injected current densities (Page 2124, right column, last paragraph)].

Regarding claim 48 Vonsovici discloses the method of claim 44, wherein said optical design portion further comprises at least one of the croup consisting of: a waveguide grating portion [Vonsovici: Figure 1, page 2124, The grating couples the light into the waveguide (Page 2124, right column second paragraph)], a diffraction optical element portion [Vonsovici: Figure 1, page 2124, The grating couples the light into the waveguide via the first diffraction order and is reflected back by the FP etalon (Page 2124, right column second paragraph)], a finite difference time domain portion [Vonsovici: To get an estimation of the error we made by using this method, a comparison with the semivectorial finite difference method (SVFD) [10]–[11] has been made (Figure 1, page 2124, page 2125 right column, first full paragraph)], a thin film portion, a beam propagation method portion, and a raytracing portion [Vonsovici: Section II, page 2125, Waveguide structure].

Regarding claim 49 Vonsovici discloses the method of claim 44, wherein the computer processor operating with a computer software simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including one from the group of a focusing mirror, a waveguide, and a Fabry-Perot cavity [Vonsovici: Page 2125-2126 Section III Fabry-Pert Waveguide Interferometer].

Regarding claim 52 Vonsovici discloses the method of claim 44, wherein the computer processor operation with a computer software simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including a diode [Vonsovici: Section II, page 2125, Waveguide structure].

Regarding claim 53 Vonsovici discloses the method of claim 44, wherein the computer processor operation with a computer software simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including a transistor [Vonsovici: Section II, page 2125, Waveguide structure].

Regarding claim 54 Vonsovici discloses the method of claim 44, wherein the integrated optical/electronic circuit is at lest partially formed on a Silicon-On-Insulator (SOI) substrate [Vonsovici: First, we analyze the optical properties of the waveguide FP interferometer based on silicon-on-insulator (SIMOX) strip loaded waveguides (Page 2124, right column, second full paragraph)].

Regarding claim 55 Vonsovici discloses the method of claim 54, wherein the optical simulation design tools portion partially models a waveguide included in said at least certain optical circuits [Vonsovici: Page 2125-2126 Section III Pafry-Perot Waveguide Interferometer].

Regarding claim 56 Vonsovici discloses the method of claim 55, wherein said SOI substrate includes a substrate later, and wherein said waveguide at least partially extends within said substrate layer [Vonsovici: Figure 2, Page 2125].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. Claims 50 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vonsovici as applied to claim 44 above, and further in view of "Integrated optical directional couplers in silicon-on-insulator" by P.D. Trinh et al., hereinafter "Trinh".

Regarding claim 50 Vonsovici teaches the method of claim 44, wherein the computer processor operation with a computer software simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including various optical characteristics of integrated optical/electronic circuits. [Vonsovici: Section II, page 2125, Waveguide structure].

Vonsovici does not expressly teach that the optical characteristics of an integrated optical/electronic circuit as including a wavelength division multiplexer modulator.

Trinh teaches that wavelength division multiplexer modulators are part of SOI optoelectronic devices [Trinh: Page 2097, left column, first paragraph], and that simulation is used to obtain the optical characteristics [Page 2097, right column, first full paragraph].

It would have been obvious to a person of ordinary skill in the art at the time of Applicant's invention to combine the simulation and method of Vonsovici with the technology and structure of Trinh.

The motivation for doing so would have been the technical advantage as described by Trinh

> [Silicon-on-insulator (SOI) technology holds great promise for advancing the performance of CMOS electronic circuits. Major efforts aimed at insertion of this technology are currently in progress and it is expected that SOI-CMOS electronics will be in production in the near future. The unique optical properties of SOI structures offers the ability to integrate photonic devices into CMOS integrated circuit (IC) technology. E.g. single mode waveguides with low propagation loss have been demonstrated in SiO,iSiiSiO, structures [1]. Therefore, significant incentives exist for the development of optical and optoelectronic devices in SOI technology (Page 2097, left column, first paragraph)].

8. Claim 51 is rejected under 35 U.S.C. 103(a) as being unpatentable over Vonsovici as applied to claim 44 above, and further in view of "Advances in Silicon-on-Insulator Optoelectronics" by B. Jalali et al., hereinafter "Jalali".

Regarding claim 51 Vonsovici teaches the method of claim 44, wherein the computer processor operation with a computer software simulates the operation of the optical characteristics of an integrated optical/electronic circuit as including various optical characteristics of integrated optical/electronic circuits. [Vonsovici: Section II, page 2125, Waveguide structure].

Vonsovici does not expressly teach that the optical characteristics of an integrated optical/electronic circuit as including an evanescent coupler.

Jalali teaches that evanescent coupling is an important factor when making SOI integrated optical/electronic circuits [Jalali: page 943, left column, second full paragraph].

It would have been obvious to a person of ordinary skill in the art at the time of Applicant's invention to combine the simulation and method of Vonsovici with the simulation and method of Jalali.

The motivation for doing so would have been as described by Jalali that evanescent coupling is a preferred method for integration of integrated optical/electronic circuits [Jalali: page 943, left column, second full paragraph].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luke Osborne whose telephone number is (571) 272-4027. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Paul L. Rodriguez can be reached on (571) 272-3753. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

LRO

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